South Sea Semiconductor

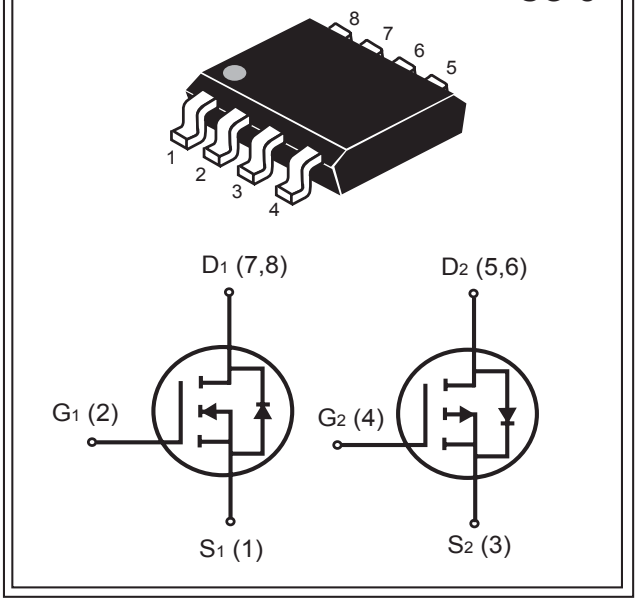
SSM8445

Dual Enhancement Mode MOSFET

Product Summary (N-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
40V	6.8A	30 @V_{GS} = 10V
		45 @V_{GS} = 5V
		50 @V_{GS} = 4.5V

Product Summary (P-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
- 40V	- 4.8A	58 @V_{GS} = - 10V
		95 @V_{GS} = - 5V
		115 @V_{GS} = - 4.5V

SO-8



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter		Symbol	N-Channel Limited	P-Channel Limited	Unit
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	
Drain Current-Continuous @ Ta	25 °C	I_D	6.8	-4.8	A
	70 °C		5.5	-4.0	
-Pulsed [b]		I_{DM}	30	-20	
Drain-Source Diode Forward Current [a]		I_S	1.6	-1.6	
Maximum Power Dissipation [a]	Ta=25 °C	P_D	2.0		W
	Ta=70 °C		1.44		
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

THERMAL CHRACTERISTICS

Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62.5	°C/W

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N-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=32V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6.0A		25	30	mΩ
		V_{GS}=5V, I_D=5A		35	45	
		V_{GS}=4.5V, I_D=4.5A		40	50	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=5V, V_{GS}=4.5V	20			A
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=6.6A		10		S
Input Capacitance	C_{ISS}	V_{DS}=15V			800	pF
Output Capacitance	C_{OSS}	V_{GS}=0V			150	
Reverse Transfer Capacitance	C_{RSS}	f=1.0MHz			110	
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=15V,			10	ns
Rise Time	t_r	I_D=6.6A,			35	
Turn-Off Delay Time	$t_{D(OFF)}$	V_{GS}=10V,			22	
Fall Time	t_f	R_{GEN}=3Ω			12	
Total Gate Charge	Q_g	V_{DS}=10V, I_D=6.6A, V_{GS}=10V			17	nC
		V_{DS}=10V, I_D=6.6A, V_{GS}=4.5V			9	
Gate-Source Charge	Q_{gs}	V_{DS}=15V, I_D=6.6A, V_{GS}=10V			3.5	
Gate-Drain Charge	Q_{gd}				5	
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=1.6A		0.8	1.2	V

P-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D= - 250μA	- 40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-32V, V_{GS}=0V			-1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D= - 250μA	-1	-1.9	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}= - 10V, I_D= - 4A		50	58	mΩ
		V_{GS}= - 5V, I_D= - 3.0A		85	95	
		V_{GS}= - 4.5V, I_D= - 2.5A		105	115	
On-State Drain Current	$I_{D(ON)}$	V_{DS}= - 5V, V_{GS}= - 10V	20			A
Forward Transconductance	g_{FS}	V_{DS}= - 5V, I_D= - 5A		10		S
Input Capacitance	C_{ISS}	V_{DS}=-15V V_{GS}=0V f=1.0MHz			800	pF
Output Capacitance	C_{OSS}				170	
Reverse Transfer Capacitance	C_{RSS}				110	
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}= - 15V, V_{GS}= - 10V, R_{GEN}=3Ω, R_L=2.7Ω			14	ns
Rise Time	t_r				30	
Turn-Off Delay Time	$t_{D(OFF)}$				75	
Fall Time	t_f				35	
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-5A, V_{GS}=-10V			15	nC
		V_{DS}=-15V, I_D=-5A, V_{GS}=-4.5V			9	
Gate-Source Charge	Q_{gs}	V_{DS}= - 15V, I_D= - 5A, V_{GS}= -10V			2.5	
Gate-Drain Charge	Q_{gd}				5	
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D= -1.6A		-0.8	-1.2	V

Notes：

a. Surface Mounted on FR4 Board, t ≤10 sec.

b. Pulse Test：Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

c. Guaranteed by design, not subject to production testing.

N-Channel

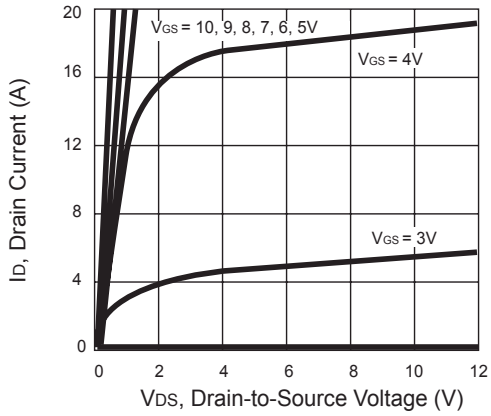


Figure 1. Output Characteristics

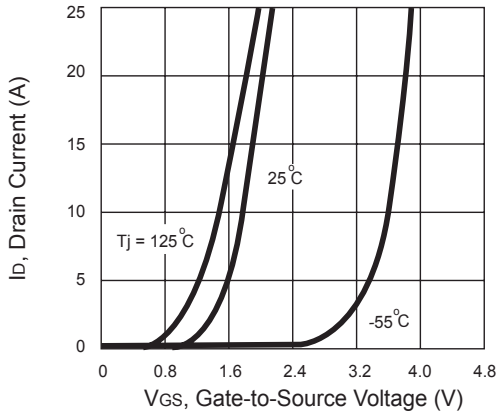


Figure 2. Thansfer Characteristics

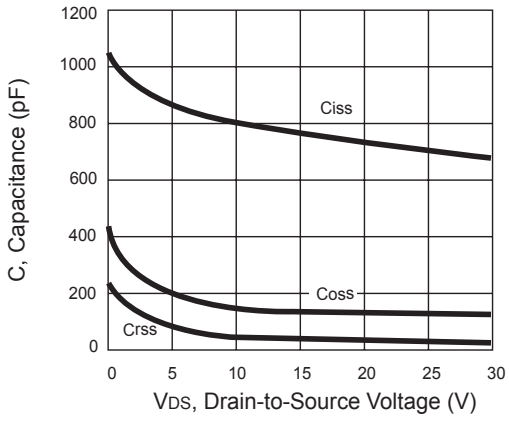
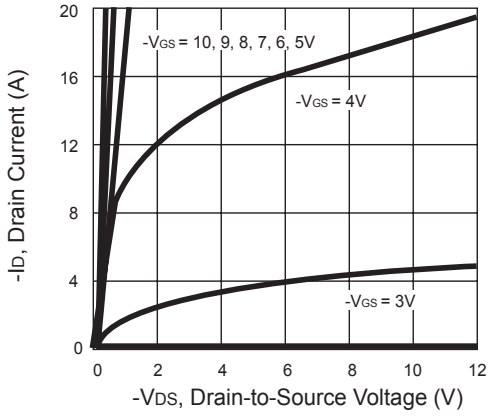


Figure 3. Capacitance

P-Channel



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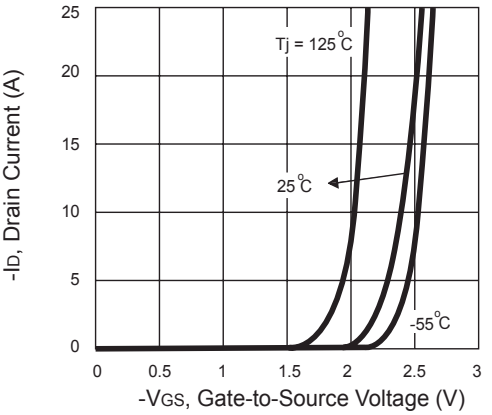

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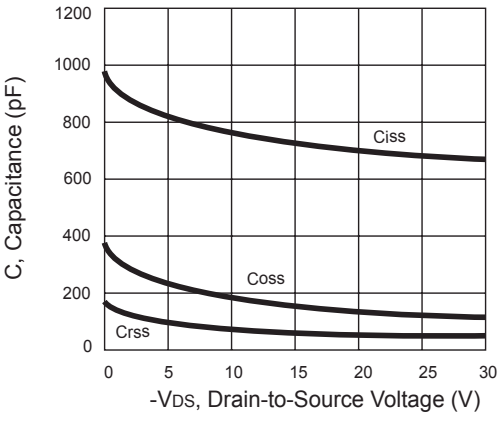

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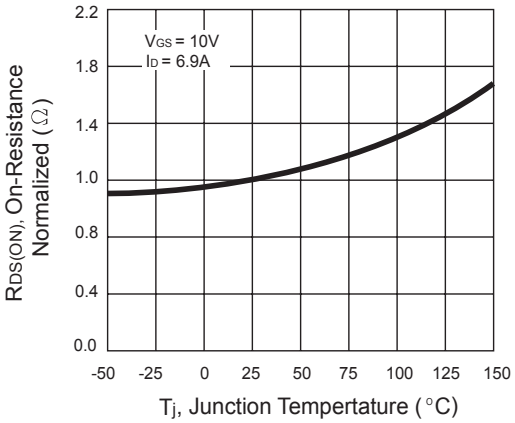


Figure 4. On-Resistance Variation with Temperature

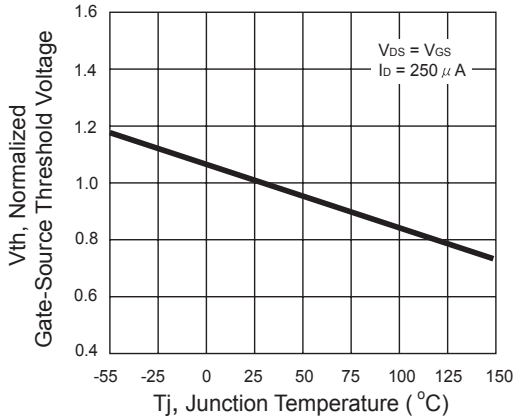


Figure 5. Gate Threshold Variation with Temperature

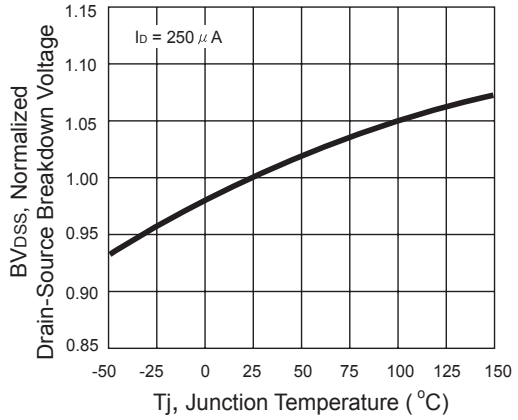
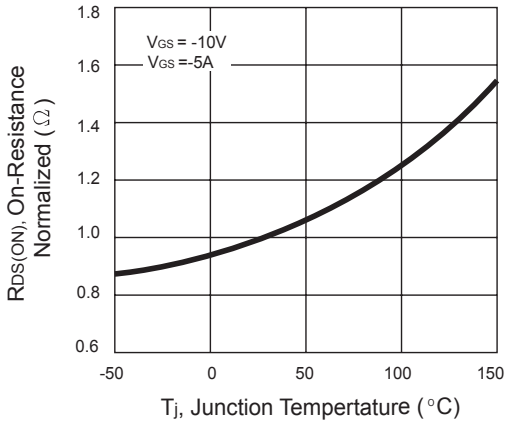


Figure 6. Breakdown Voltage Variation with Temperature

P-Channel



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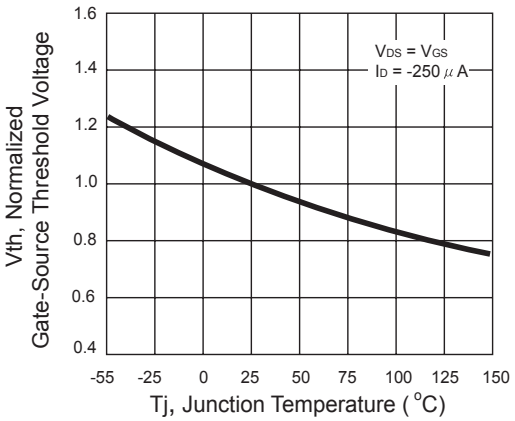

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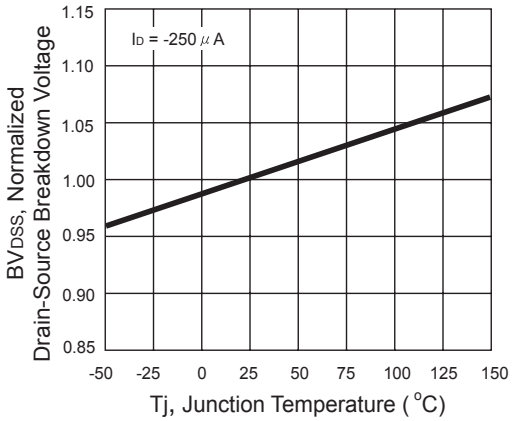

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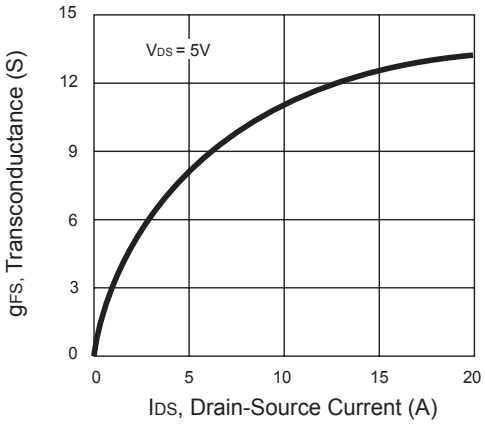


Figure 7. Transconductance Variation with Drain Current

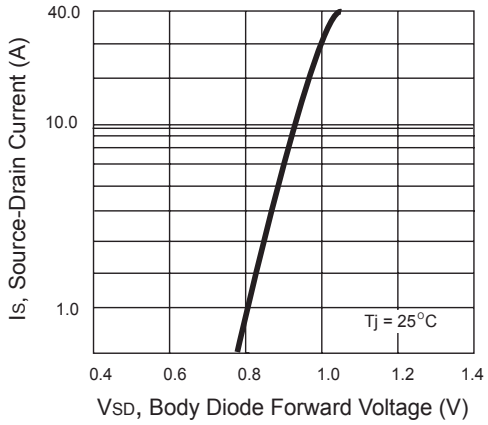


Figure 8. Body Diode Forward Voltage Variation with Source Current

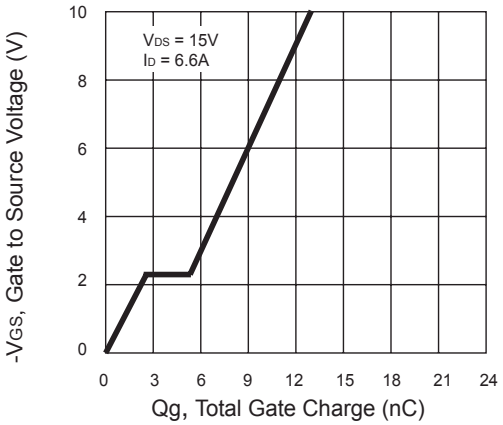
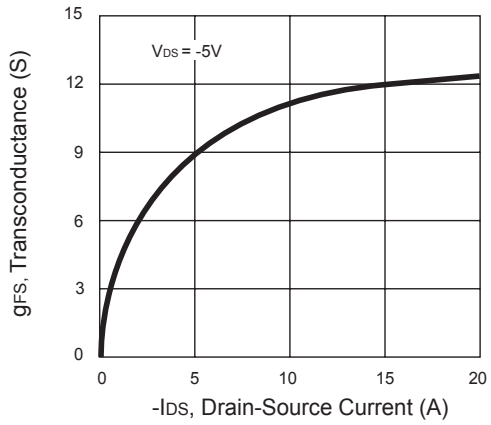


Figure 9. Gate Charge

P-Channel



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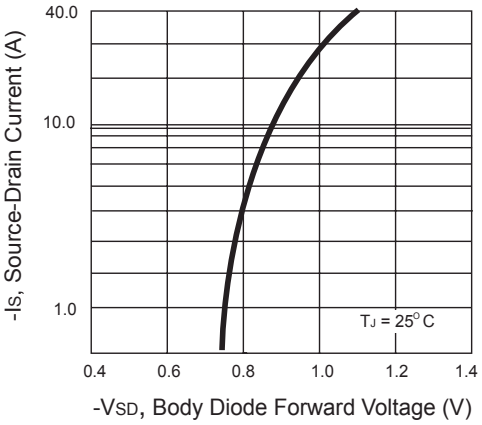

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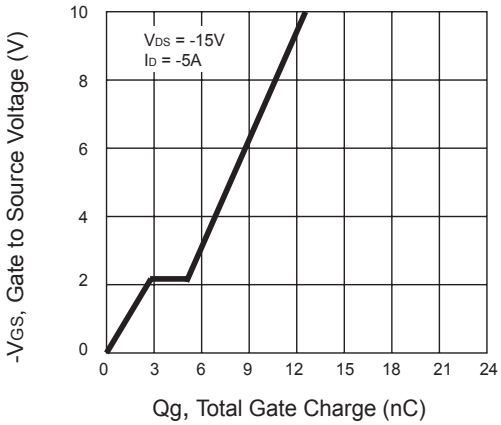

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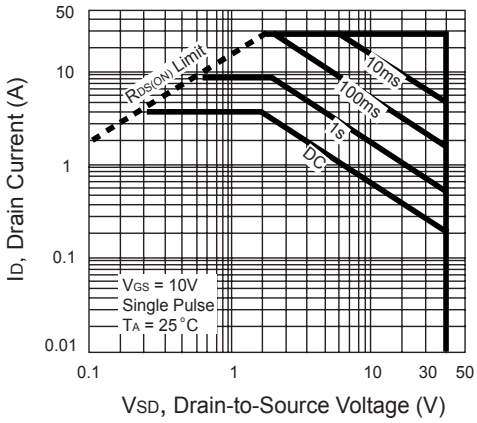
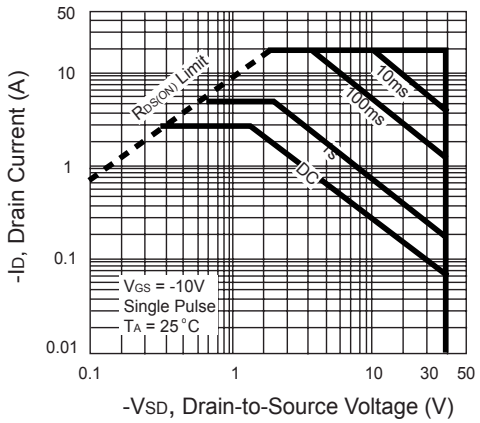


Figure 10. Maximum Safe Operating Area

P-Channel



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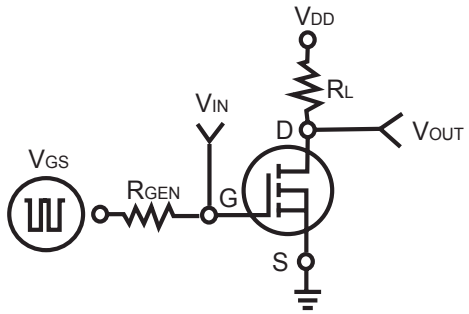


Figure 11. Switching Test Circuit

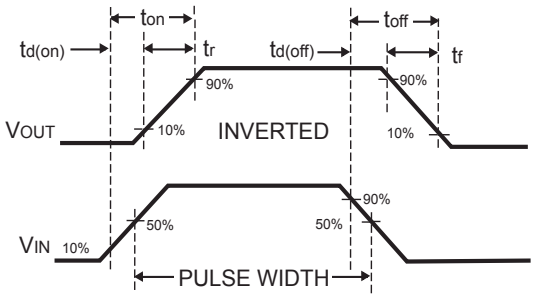


Figure 12. Switching Waveforms

N-Channel

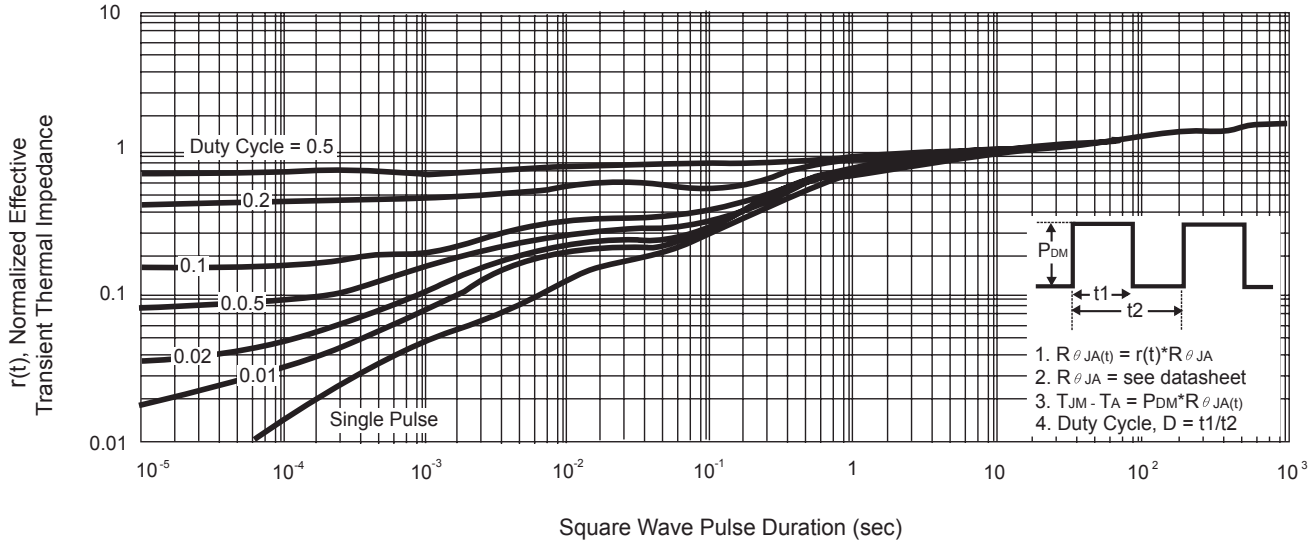
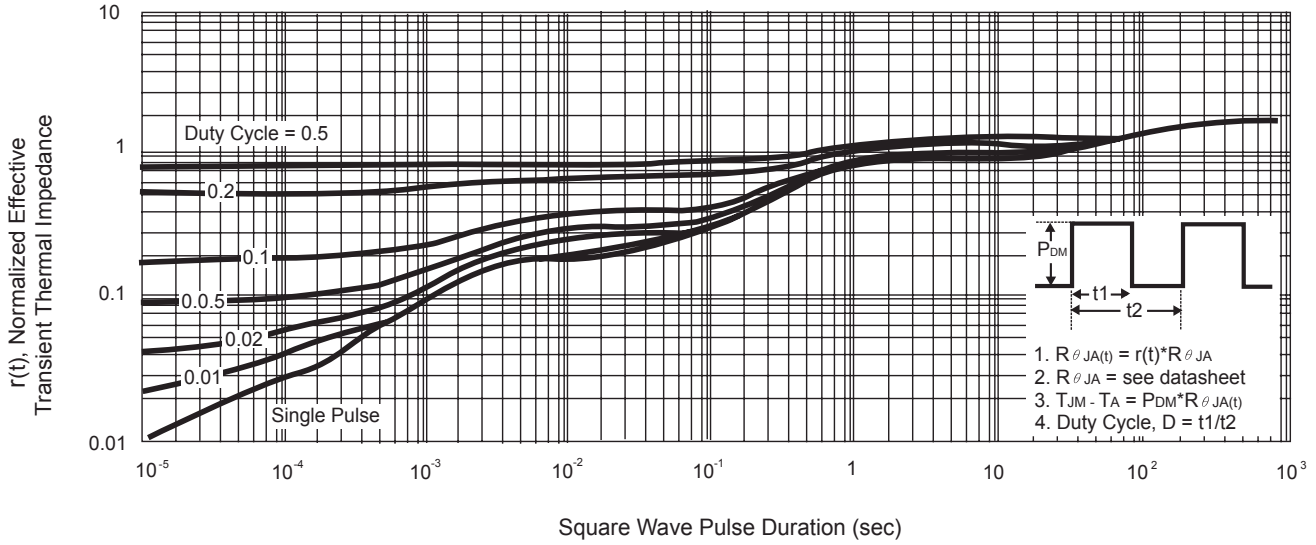


Figure 13. Normalized Thermal Transient Impedance Curve

P-Channel



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