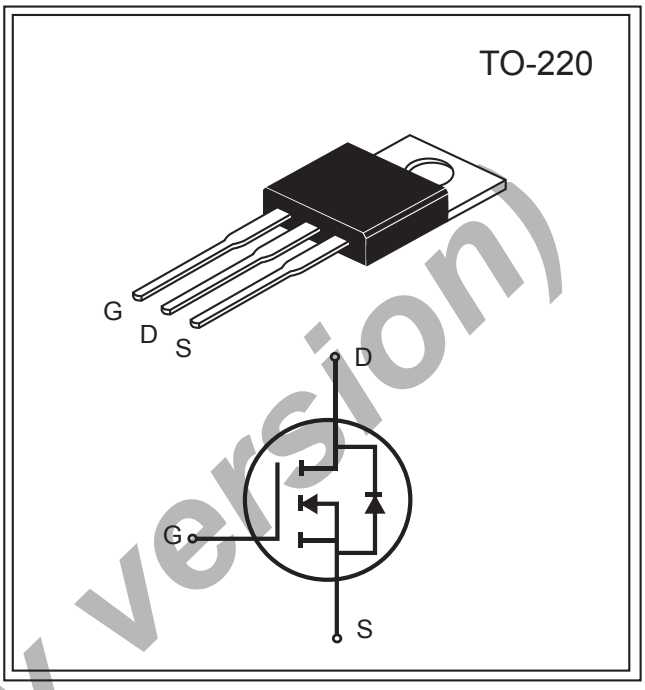
South Sea Semiconductor

SSP4070NL

N-Channel Enhancement Mode MOSFET

Product Summary		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
70V	40A	50 @V_{GS} = 10V
		80 @V_{GS} = 5V



FEATURES

- Super high density cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- TO-220 package.
- Pb free.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	70	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous @ T_C = 25°C	I_D	40	A
-Pulsed [b]	I_{DM}	100	A
Drain-Source Diode Forward Current [a]	I_S	20	A
Maximum Power Dissipation[a] @T_C = 25°C	P_D	75	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.0	°C/W
Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62	

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Electrical Characteristics (T_A = 25℃ unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	70			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.8	3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=25A		42	50	mΩ
		V_{GS}=5V, I_D=15A		72	80	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=10V, V_{GS}=10V	40			A
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=15A		9		S
Input Capacitance	C_{ISS}	V_{DS}=25V V_{GS}=0V f=1.0MHz		1100		pF
Output Capacitance	C_{OSS}			160		
Reverse Transfer Capacitance	C_{RSS}			60		
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=30V, I_D=20A, V_{GS}=10V, R_{GEN}=6Ω		30		ns
Rise Time	t_r			80		
Turn-Off Delay Time	$t_{D(OFF)}$			27		
Fall Time	t_f			40		
Total Gate Charge	Q_g	V_{DS}=30V, I_D=20A, V_{GS}=5V		8		nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2.5		
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=20A			1.4	V

Notes：

a. Surface Mounted on FR4 Board, t ≤10 sec.

b. Pulse Test：Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

c. Guaranteed by design, not subject to production testing.

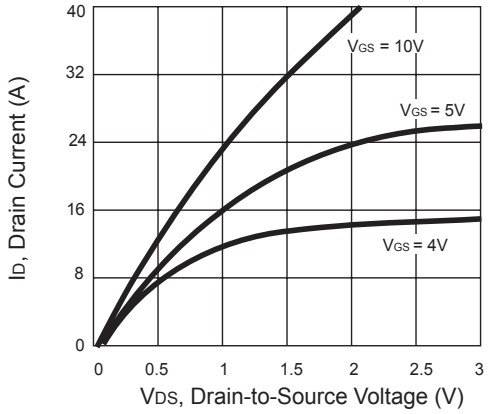

Figure 1. Output Characteristics

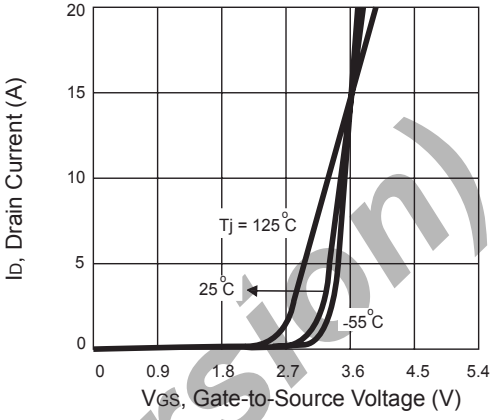

Figure 2. Thansfer Characteristics

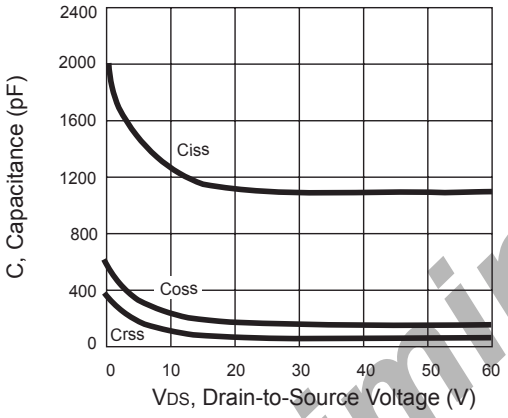

Figure 3. Capacitance

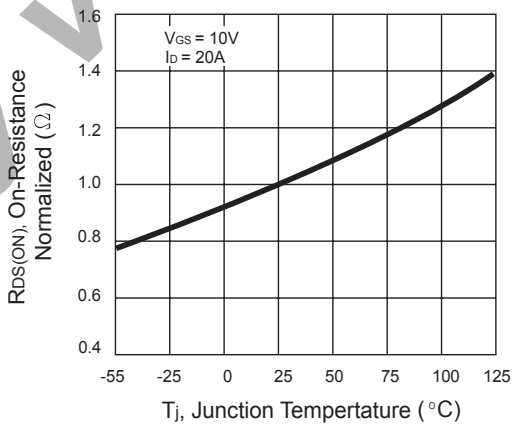

Figure 4. On-Resistance Variation with Temperature

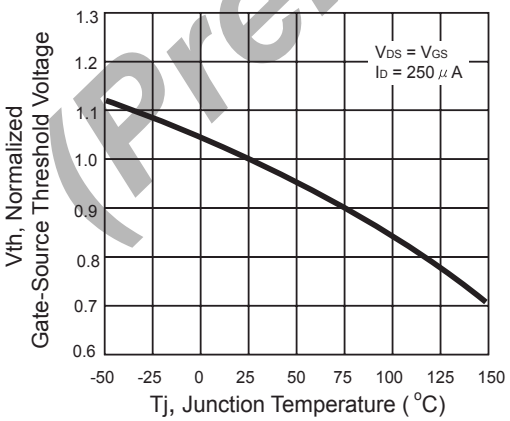

Figure 5. Gate Threshold Variation with Temperature

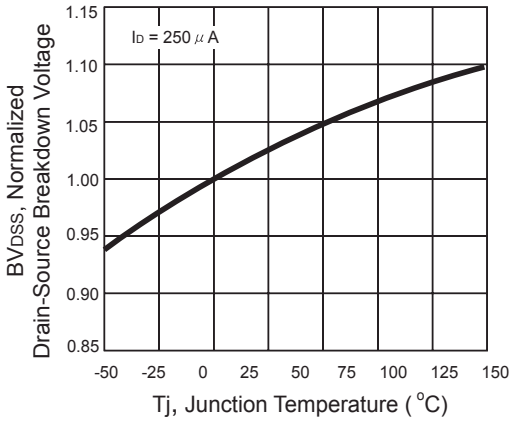

Figure 6. Breakdown Voltage Variation with Temperature

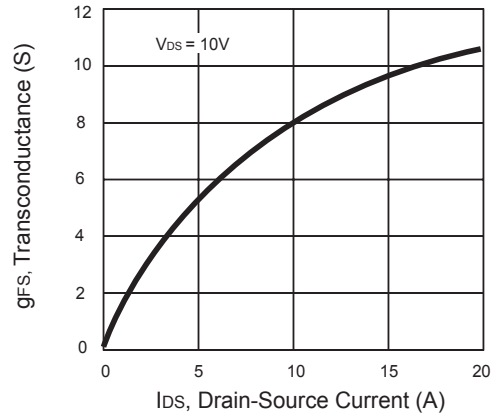

Figure 7. Transconductance Variation with Drain Current

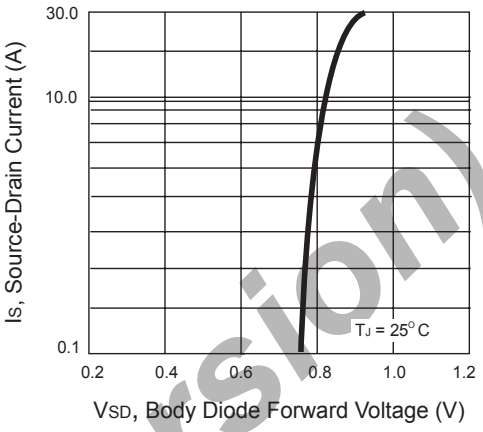

Figure 8. Body Diode Forward Voltage Variation with Source Current

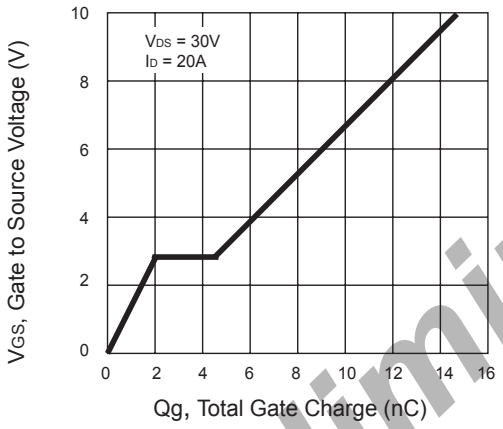

Figure 9. Gate Charge

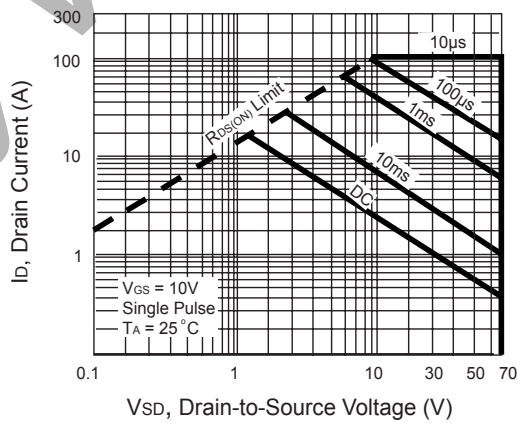

Figure 10. Maximum Safe Operating Area

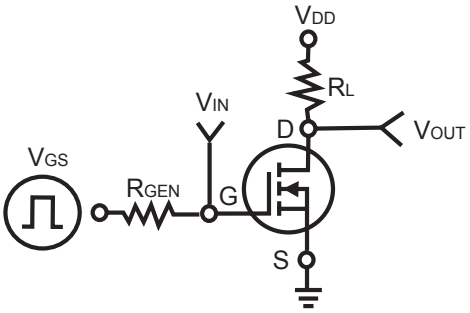

Figure 11. Switching Test Circuit

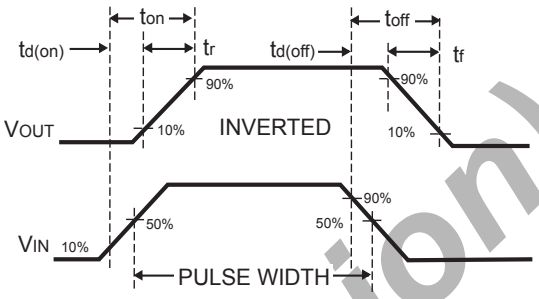

Figure 12. Switching Waveforms

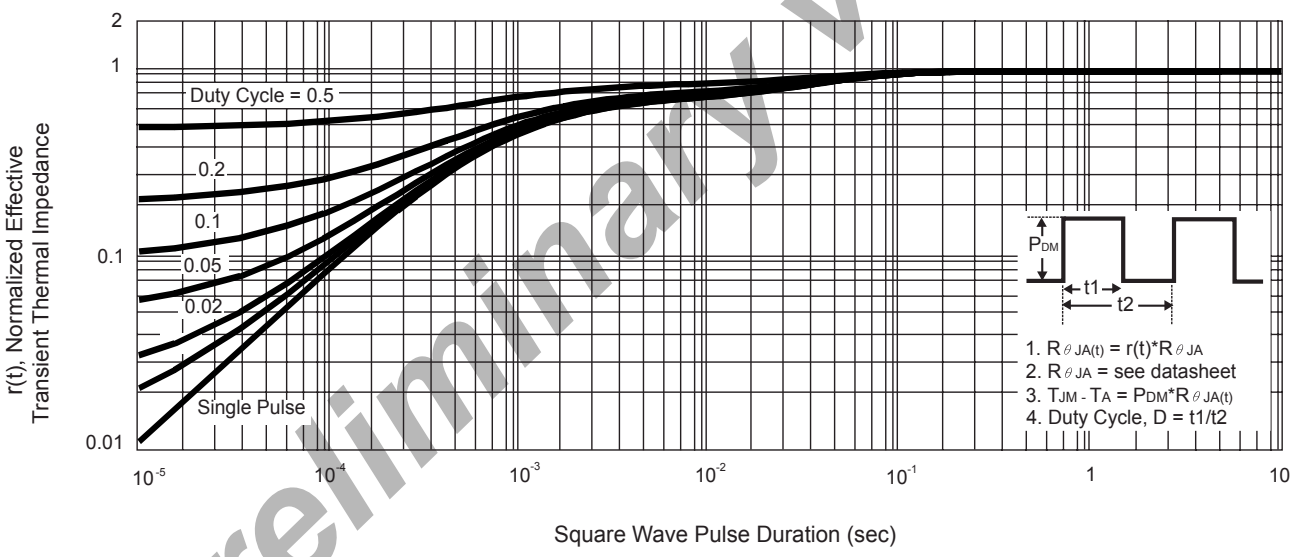

Figure 13. Normalized Thermal Transient Impedance Curve